ABSTRACT

A first differential amplifier circuit includes a first P-type transistor and a second P-type transistor which constitute a current mirror circuit, and operates based on an input voltage V_{IN}. A second differential amplifier circuit includes a first N-type transistor and a second N-type transistor forming a current mirror circuit and operates based on the common input voltage V_{IN}. A third P-type transistor operable based on a first signal S1 from the first differential amplifier and a third N-type transistor operable based on a second signal S2 from the second differential amplifier are provided. A voltage between these third P-type and third N-type transistors becomes an output voltage V_{OUT}. The first differential amplifier circuit has a fourth N-type transistor that is connected in series to the first P-type transistor and a fourth N-type transistor connected in series to the second P-type transistor, wherein a driving ability difference is provided between a pair of transistors forming a first differential pair.